Jessen 7-1-4

Election #5/A 11/21/02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Application of:

Scott Jessen, *et al.*

Serial No.: 09/966,157

Filed: 09/28/2001

Title: MASK LAYER AND INTERCONNECT STRUCTURE FOR DUAL DAMASCENE SEMICONDUCTOR MANUFACTURING

Group Art Unit: 2822

Examiner: Maria F. Guerrero

Commissioner for Patents
Box Fee Amendment
Washington, DC 20231

RESPONSE

The paper is submitted in response to the Office Action mailed June 6, 2002, for which a response was due by July 6, 2002.

RESTRICTION

The Applicant herein responds to the restriction requirement in the above-reference Office Action wherein the Applicant restricts the application to claims 6 through 20 for the purpose of examination. Applicant makes this restriction with traversal, which is set forth in detail in the below Remarks.

AMENDMENT

Please add the following claims:

A1 Sub 047

21. (Added) A method for the fabrication of a semiconductor device including a wafer substrate having a dielectric material formed over a metallization layer formed over said wafer substrate, comprising the steps of: